

CLAIMS:

SWB/AF

1. An integrated circuit comprising:
a processor core;
a configurable peripheral device; and
a bus connecting said processor core and said
configurable peripheral device.
2. The integrated circuit of claim 1 wherein said
peripheral device is a universal asynchronous receiver
transmitter (UART).
3. The integrated circuit of claim 2 wherein said UART has
a fixed baud rate.
4. The integrated circuit of claim 1 wherein said processor
core, said configurable peripheral device and said bus are
implemented on a field programmable gate array.
5. The integrated circuit of claim 1 wherein said
peripheral device is a flash memory controller.
6. A system allowing a user to select peripheral devices in
a programmable logic device, comprising:
a menu system allowing said user to select one of a
plurality of peripheral devices; and
an integrated circuit comprising:
a processor core;
a configurable peripheral device corresponding to said
one peripheral device selected using said menu system; and
a bus connecting said processor core and said
configurable peripheral device.

7. The system of claim 6 wherein said configurable peripheral device is a universal asynchronous receiver transmitter (UART).

8. The integrated circuit of claim 7 wherein said UART has a fixed baud rate.

9. The integrated circuit of claim 6 wherein said configurable peripheral device is a flash memory controller.

ACDM

2025 RELEASE UNDER E.O. 14176